ABSTRACT OF THE DISCLOSURE

The present invention facilitates clock and data recovery for serial data streams by providing a mechanism that can be employed to detect and adjust operation and timing of clocks. The invention employs a differential analog circuit, using current steering logic, to process center and edge samples and identify an average operation of the clocks. The circuit can identify transitions between adjacent center/edge data samples and determine whether an identified transition is early or late for each bit in a set of consecutive bits of a received serial data stream.